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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,931	07/10/2001	Kirk Martin	NTG-P101	9250

32566 7590 07/30/2003

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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 07/30/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/902,931

Applicant(s)

MARTIN, KIRK

Examiner

Lan Vinh

Art Unit

1765

-- Th MAILING DATE of this communication app ars on th cover sheet with the correspondenc address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 2-12 and 14-37 is/are pending in the application.
- 4a) Of the above claim(s) 22-28, 34 and 37 is/are withdrawn from consideration.
- 5) ☐ Claim(s) 14-21, 29-33 and 36 is/are allowed.
- 6) ☒ Claim(s) 2-6, 10-12 and 35 is/are rejected.
- 7) ☒ Claim(s) 7-9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Newly submitted claim 37 and originally filed claims 22-28, 34 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 22-28, 34 and 37, drawn to an apparatus for etching a semiconductor dielectric whereas originally claims 1-21, 29-33 drawn to a method for etching a semiconductor dielectric.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 22-28, 34 and 37 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

2. For the purpose of examination, the claim language of "a thickness less than about 0.5 mm" is best understood by the examiner as a thickness less than 0.5 mm. The term "inactive surfaces" are defined in page 5 and fig. 2 of the specification as a back surface of the semiconductor die.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 5, 12, 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Ellerson et al (US 5,252,179)

Ellerson discloses a method for etching an epoxy encapsulated chip/dielectric. This method comprises the steps of:

- providing an etching apparatus/assembly including substrate 10/support member and diaphragm 20/adaptor member (col 2, lines 44-55)

- placing/positioning the semiconductor chip/dielectric 11 on the support member 10 (fig. 3, fig. 3 also shows that the upper/exposed surface of the semiconductor die/chip 11 faces away from the support member 10

- positioning diaphragm 20/adaptor member adjacent the upper/exposed surface of the chip 11 to form a channel between the upper/exposed surface of the chip/die 11 and the adaptor member 20 (fig. 3)

- flowing an etchant into fluid channel 22 diverted into cavity 23 across the upper/exposed surface of the chip/die 11 to etch the chip (col 3, lines 30-32, fig. 3 ), which reads on flowing an etchant through the channel across the exposed surface from the first edge to the second edge to etch the semiconductor dielectric

Regarding claim 5, Ellerson discloses that the flowing of the etchant is performed in a closed/sealed chamber formed by the support member 10 and adaptor member 20 (fig. 3)

Regarding claim 12, as shown in fig. 2 of Ellerson, the upper/exposed surface of chip 11 is disposed within a cavity formed in an encapsulant 13.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2,11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellerson et al (US 5,252,179) in view of Gigante (US 4,372,803)

Ellerson method has been described above. Although Ellerson discloses flowing an acidic etchant through the channel, Ellerson does not specifically disclose using an etchant comprises of nitric acid, hydrofluoric acid and acetic acid.

However, Gigante discloses a method for etch thinning silicon device comprises the step of flowing an etching mixture of hydrofluoric acid, nitric acid and acetic acid to etch the chip, the etching mixture is mixed in a spherical mixing chamber 22 (col 2, lines 41-42, fig. 5-6)

Since Ellerson is concerned with a step of etching the exposed surface of the chip, one skilled in the art would have found it obvious to modify Ellerson's etching step by using an etching mixture as per Gigante because according to Gigante, the etching mixture of hydrofluoric acid, nitric acid and acetic acid is a thinning etchant for the semiconductor chip (col 2, lines 37-42)

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7. Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellerson et al (US 5,252,179) in view of Harris et al (US 4,359,360)

Ellerson's method has been described above in paragraph 4. Unlike the instant claimed invention as per claim 3, Ellerson does not disclose the specific etchant flow rate across the exposed surface of the chip/die.

However, Harris, in a method for selectively etching a encapsulating semiconductor device, teaches that the etchant flow rate can be controlled to affect the result of the etching step (col 1, lines 67-68, col 2, lines 58-60)

Thus, Harris serves as evidence that the etchant flow rate is a "result effective variable". Hence, one skilled in the art would have found it obvious to modify Ellerson by discovering the optimum values for the etchant flow rate because Harris discloses that the flow rate is a result effective variable in the same field of endeavor

Unlike the instant claimed invention the instant claimed invention as per claim 4, Ellerson does not disclose that the flow of the etchant across the exposed surface is turbulent.

Harris also discloses the step of creating turbulent flow of etchant across an encapsulating semiconductor device (see abstract)

Hence, one skilled in the art would have found it obvious to use a turbulent flow of etchant across Ellerson exposed chip/die surface to result in complete etching as taught by Harris (col 1, lines 67-68)

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8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellerson et al (US 5,252,179) in view of Miller (US 5,064,498)

Ellerson's method has been described above in paragraph 4. Unlike the instant claimed invention as per claim 6, Ellerson does not specifically disclose flowing an acidic solution comprises HF to partially remove oxide on the exposed surface.

However, Miller discloses a method for backside etch for semiconductor device comprises the step of using an acidic solution comprises HF to remove oxide on the exposed surface of the die (col 2, lines 53-55 )

Since Ellerson is related to a method of flowing etchant across the exposed surface, one skilled in the art would have found it obvious to modify Ellerson's method by flowing an acidic solution comprises HF to partially remove oxide on the exposed surface of the die in view of Miller teaching to enhances failure analysis of the dielectric/chip by allowing engineer to keep the memory structure of the chip intact (col 2, lines 40-44)

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellerson et al (US 5,252,179) and further in view of Muller (US 5,956,142)

Ellerson's method has been described above in paragraph 4. Although Ellerson discloses flowing a layer of etchant across the exposed surface of the die, Ellerson does not disclose the specific thickness of the etchant layer as recited in claim 9.

However, Muller, in a wet etching method, discloses that the thickness of the liquid/etchant layer is variable (col 5, lines 13-15 ) and varying liquid etchant layer thickness effects the progress of etching (col 4, lines 22-25 )

Thus, Muller serves as evidence that the liquid etchant layer thickness is a "result effective variable". Hence, one skilled in the art would have found it obvious to modify Ellerson by discovering the optimum values for the thickness of the etchant layer because Muller discloses that the thickness of the etchant layer is a result effective variable in the same field of endeavor

***Allowable Subject Matter***

10. Claims 14-21, 29-33, 36 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 29, the cited prior art of record fails to disclose the step of inserting a first surface of a first member into the cavity to form a channel between the first surface of the first member and the inactive surface of the semiconductor die. The closest prior art of Ellerson et al (US 5,252,179) discloses the step of inserting a surface of movable housing 70/first member into the cavity 23 to form a channel 22 between a surface of the first member and the diaphragm holder 30 on the side of semiconductor die 11 (fig. 3 )

Regarding claim 36, the cited prior art of record fails to disclose the step of flowing a second acidic solution through the channel across the second surface of the semiconductor dielectric to at least partially polish the second surface of the semiconductor die. The closest prior art of record of Ellerson et al (US 5,252,179) discloses flowing an etchant into fluid channel 22 diverted into cavity 23 across the

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upper/exposed surface of the chip/die 11 for only one cycle to etch the chip without suggesting flowing a second acidic solution through the channel.

Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 7-9, the cited prior art of record fails to disclose the step of flowing an acidic solution through the channel across the exposed surface of the die preceding/subsequent to the flowing of the etchant through the channel. The closest prior art of record of Ellerson et al (US 5,252,179) discloses flowing an etchant into fluid channel 22 diverted into cavity 23 across the upper/exposed surface of the chip/die 11 for only one cycle to etch the chip without suggesting flowing additional acidic solution through the channel preceding/subsequent to the flowing of the etchant through the channel.

### ***Response to Arguments***

11. Applicant's arguments with respect to claims 2-6, 10-12, 35 have been considered but are moot in view of the new ground(s) of rejection.

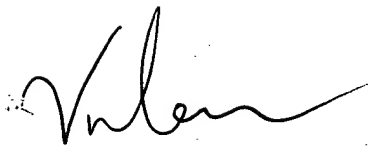
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***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

A handwritten signature in black ink, appearing to read 'Lan Vinh', with a stylized, flowing script.

LV  
July 25, 2003